FD SOI technology

Advantages

- negligible drain to sub cap
- No latch up (no wells to act as a base)
- Ideal n+/n+ & p+/p+ isolation
- Improved SER
- Reduced junction lkg
- Steeper Sub-threshold slope (see appendix)
- Positive body bias effect
- Improved SCE (no deep punch through)
- Butted junction for n+/p+ strap

Disadvantages

- Dynamic floating body effect caused by impact ionization results in dynamic Vt
  - FD SOI suppresses the kink effect
- Self heating (Si is a good thermal conductor, SiO2 is not)
- Body bias knob not available without significant area penalty

MITLL180_XLP Technology

Mesa Si islands (edge effect)

1.6.4. Edge Effects. Since the MITLL FDSOI process is mesa isolated, the standard NMOS and PMOS devices illustrated in Figs. 1-2 through 1-4 each include parasitic MOS devices at the island edges. A schematic cross section of a typical parasitic "edge" device is shown in Fig. 1-5. These devices result in poor threshold voltage control. In addition, some tests have shown that edge devices may have substantially increased low-frequency noise. In the majority of MITLL FDSOI process versions, edge effects are minimized through the use of a sidewall implant. It is important for the designer to understand that post-processing of layout data will be performed in order to create the appropriate sidewall implant masks.

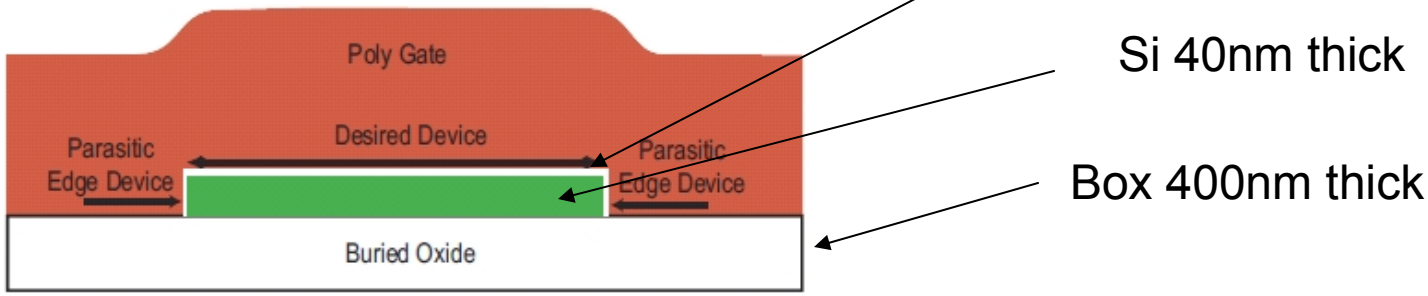
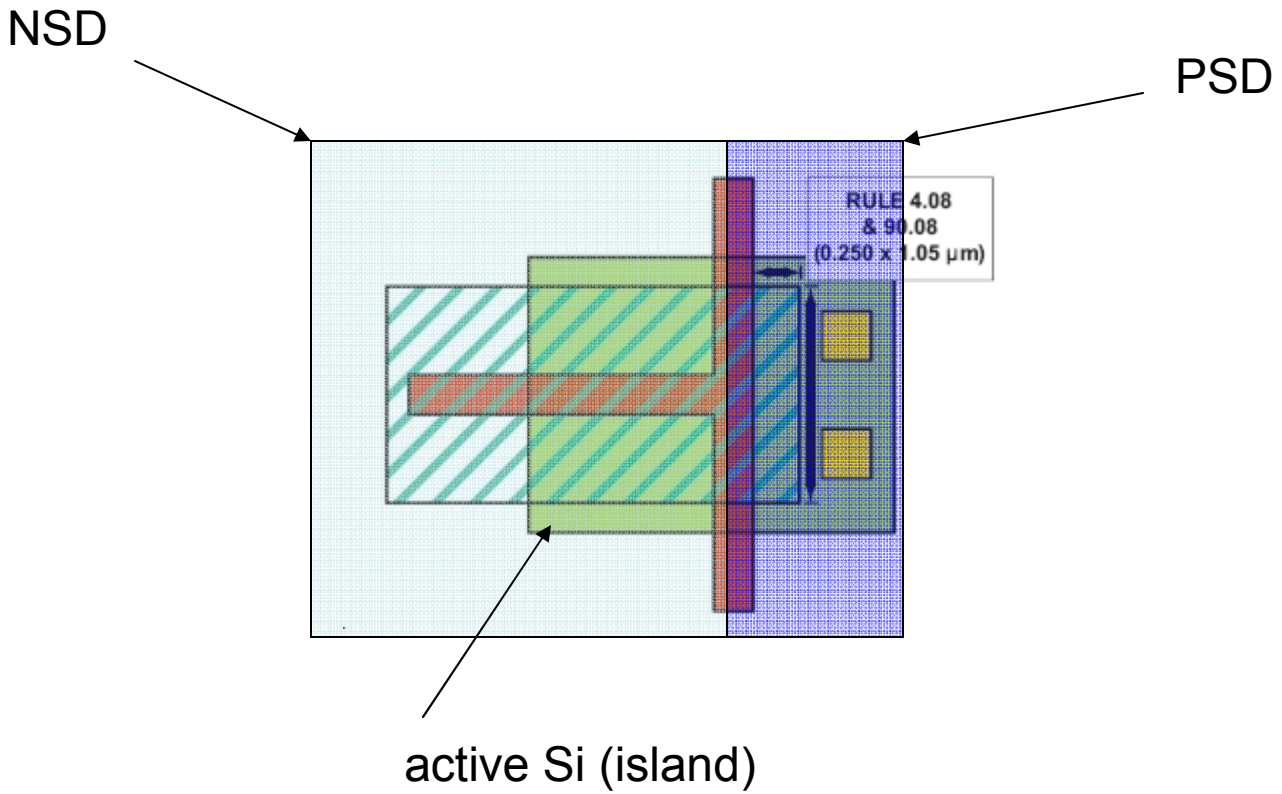


Figure 1-5: Cross section of parasitic edge device.

In addition, it should be understood that edge effects can be completely eliminated by designing with devices that have no edge as drawn. See the section "Special Purpose MOS Structures" for more information on edgeless devices.

Method for forming a body contact on SOI structures



Butted junction

1.7.4. Abutting Devices. Since all exposed active and poly surfaces are silicided following poly deposition, abutting devices of opposite types may be used to save area, as illustrated in Fig. 1-11.

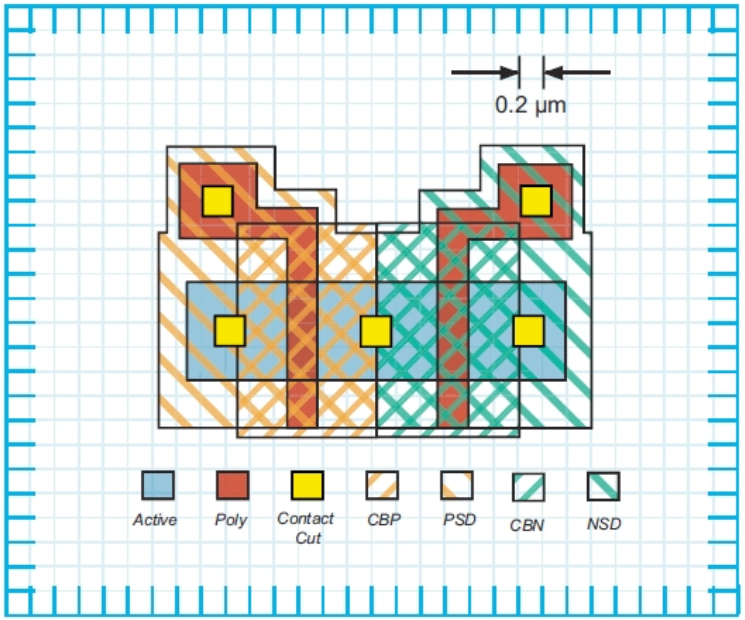
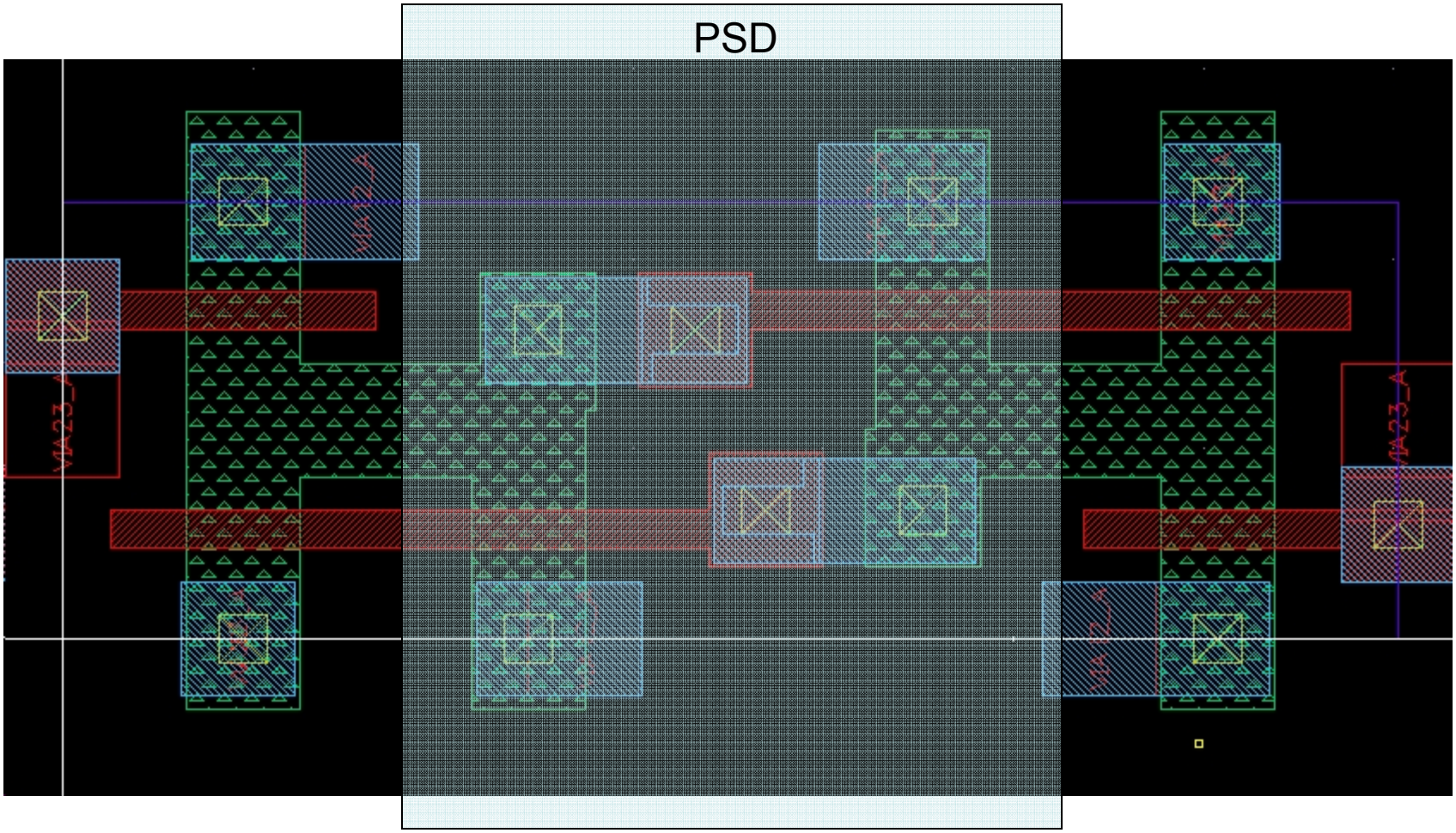


Figure 1-11: Abutting NMOS and PMOS devices. W = 0.80 µm, L = 0.25 µm.

In tests to date MITLL has seen no effect of such abutting active regions as long as they are at least 0.4 µm from the channel. Yield of such devices, however, has not been characterized by testing large numbers, so their use entails some risk.

SRAM layout example using the butted junction



MITLL 180 XLP technology (fully depleted SOI)

XLP Technology overview

- 1.5V and 0.3V with 4nm Tox (note std Tox is 2.5nm)
- Silicided diffusion and poly for Rs ~13 Ohm/sq
- Silicide block level for Resistor
- (20nmTiN/200nm poly) gate stack
- 40nm Si/400nm BOX
- Min L=0.15um, Min W=0.5um (device)
- 0.025um design grid
- 3LM technology

Technology Summary

Overview of key technology GRs

- min L = 0.15um over active
- min L = 0.2um over field (thick ox)
- min W = 0.5um
- Cont = 0.25x0.25um
- Cont-Cont spacing=0.35um
- Cont-gate = 0.35um for XLP (0.275um for non-XLP)
- Cont border (active and gate) = 0.175um
- act-act space= 0.3um
- gate past active=0.4um
- poly- poly space for XLP1 0.3V devices = 0.35um
- active past gate =0.5um
- M1-M3 pitch=0.55um (0.25um line, 0.3um space)
- Vias = .3x.3um with 0.4um spacing

Mask layers described in design guide (for single oxide thickness process)

- ACT= defines silicon islands
- CBP = p-chan Vt adjust
- CBP2=p-chan Vt for LP (higher Vt) – **not allowed in XLP**
- CBN = n-chan Vt adjust (~5E17 boron/cm3)
- CBN2= n-chan Vt adjust for LP (higer Vt) – **not allowed in XLP**
- POLY= defines gate region and poly interconnect
- NOSLC = defines silicide block region (leaves Si3N4 spacer material)
- NSD= NFET source drain implant
- PSD= PFET source drain implant
- CON= contact
- M1,M2,M3 = metal levels

Appendix

Calculation of sub-threshold slope

$$Ss(T) = \frac{k \cdot T}{q} \cdot \ln(10) \qquad Ss(T) = 59.608\text{mV}$$

$$m = 1$$

$$Ss(T) = \frac{k \cdot T}{q} \cdot \ln(10) \cdot (m)$$

$$m(Tox, Na, T) = 1 + \frac{\varepsilon si}{\varepsilon ox} \cdot \frac{Tox}{Xd(T, Na)}$$

$$Ss(Tox, Na, T) = \frac{k \cdot T}{q} \cdot \ln(10) \cdot m(Tox, Na, T)$$

$$Ss\left(4\text{nm}, \frac{3 \cdot 10^{17}}{\text{cm}^3}, 300\text{K}\right) = 0.071\text{V}$$

For FD SOI

$$msoi = 1 + \frac{Cs}{Coxi}$$

$$Cs = \frac{Csoi \cdot Cbox \cdot Csub}{Csoi \cdot Cbox + Cbox \cdot Csub + Csub \cdot Csoi}$$

$$Ssoi(Tox, Na, T) = \frac{k \cdot T}{q} \cdot \ln(10) \cdot msoi$$

$$Ssoi(Tox, Na, T) = 0.06\text{V}$$